Claims:

1. A device, comprising:

N I/O lines, wherein N is an integer;

N internal networks;

N internal multiplexers for routing signals from individual I/O lines to individual internal networks in response to control signals; and

a multiplex controller for producing said control signals.

2. A device according to claim 1, wherein at least one multiplexer is an N-to-1 multiplexer.

3. A device according to claim 1, wherein at least one multiplexer is a 2-to-1 multiplexer.

4. A device according to claim 1, wherein at least one multiplexer is a 3-to-1 multiplexer.

5. A device according to claim 1, wherein at least one multiplexer can route signals to and from N-1 multiplexers.

6. A device according to claim 5, wherein each multiplexer can route signals to an associated array.

7. A device according to claim 1, wherein a multiplexer shifts signals on an I/O line to an adjacent multiplexer.

8. A memory device, comprising:

N I/O lines, wherein N is an integer;

N addressable arrays;

N multiplexers for routing signals from individual I/O lines to said addressable arrays in response to control signals; and

a multiplex controller for producing said control signals.

9. A memory device according to claim 8, wherein at least one multiplexer is an N-to-1 multiplexer.

10. A memory device according to claim 8, wherein at least one multiplexer is a 2-to-1 multiplexer.

11. A memory device according to claim 8, wherein at least one multiplexer is a 3-to-1 multiplexer.

12. A memory device according to claim 8, wherein at least one multiplexer can route signals to and from N-1 multiplexers.

13. A memory device according to claim 12, wherein each multiplexer can route signals to an associated array.

14. A memory device according to claim 8, wherein a multiplexer shifts signals on an I/O line to an adjacent multiplexer.

15. A computer, comprising:

a processor having at least W I/O lines;

a bus for transferring at least W I/O bits to and from said processor;

a memory module attached to said bus, said memory module for storing and saving a W-bit wide word, wherein said W-bit wide word is applied to said bus, wherein said memory module is comprised of a plurality of memory devices having more than W I/O lines, wherein at least one memory device has a spare I/O line that is not connected to said bus, and wherein said at least one memory device includes:

said spare I/O line;

N-1 I/O lines, wherein N is an integer;

N addressable arrays, at least one of which is associated with said spare I/O line;

N multiplexers for routing signals from said N-1 I/O lines and from said spare I/O line to said addressable arrays in response to control signals; and

a multiplex controller for producing said control signals;

wherein data on at least one of said N-1 I/O line can be stored in

and/or read from said array associated with said spare I/O line.

16. A computer according to claim 15, wherein at least one multiplexer is an N-to-1 multiplexer.

17. A computer according to claim 16, wherein at least one multiplexer is a 2-to-1 multiplexer.

18. A computer according to claim 17, wherein at least one multiplexer is a 3-to-1 multiplexer.

19. A computer according to claim 15, wherein at least one multiplexer can route signals to an associated array.

20. A computer according to claim 15, wherein at least one multiplexer shifts signals on an I/O line to an adjacent multiplexer.